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8-30-2024  
ECEN 5730  
Lab 2 report

**Introduction**

This lab was a primer for PCB circuit design, and involved working with solderless breadboards, 555 timers, capacitors and resistors. The overall objective was to compare the rise and fall time of two 555 timers, one being a high speed circuit and the other being of a lesser speed, under varying conditions. Along with the rise and fall times, the frequency, duty cycle, and off/on time of the circuits were also analyzed. The two circuits would both be tested under the three conditions:

1. When the 555 timer output was not connected to any electrical load.
2. When the 555 timer output was connected to an led and 1kΩ resistor in series
3. When the 555 timer output was connected to an led and a 50kΩ resistor in series.

In order to complete the lab, knowledge of how to utilize an oscilloscope and BNC connectors was necessary. It also served as an exercise in best practices when building circuits, such as stripping wires to an appropriate length when making connections and performing basic lab safety.

**Equipment**

The circuit featured the following components:

1xlmc555 (fast timer)  
1xNE555DR (slow timer)  
1x50Ω resistor (composed of smaller resistors)  
2x36kΩ resistor   
2x0.01uf capacitor  
1x10uf capacitor  
1x8.2kΩ resistor

The following bench equipment was used:

1xbench power supply  
1xbench oscilloscope  
1xBNC coaxial cable  
2xaligator clip cable

**Methodology/Design**

Results were gathered in two stages, the first being with the slower 555 timer, and the second being with the faster 555 timer. In both stages, the following routine was used to collect the data needed:

1. Horizontally shift the waveform until the end of the initial high state of the waveform. Record the time shifted by. This is the time on.
2. Shift the waveform until at very start of next active high cycle, mark the time. This subtracted from the time high is the time low.
3. Zoom in on waveform using vertical controls, h shift waveform until the waveform is high, the time shifted by is the rise time.
4. H shift to the start of when waveform declines, mark time and repeat for when the waveform is in zero state. The difference between these two values is the fall time.

The circuit was constructed in the following configuration:

A diagram of a circuit

Description automatically generated

(circuit diagram)

A close up of a breadboard

Description automatically generated

(implementation of circuit)

The following is a few images of a zoomed in waveform when the rise time and fall time were both collected:

**A close up of a device

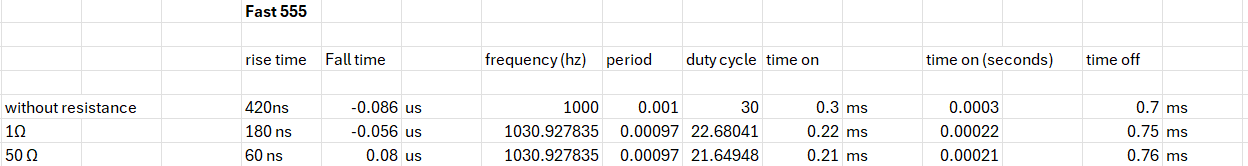
Description automatically generated**

**Results**

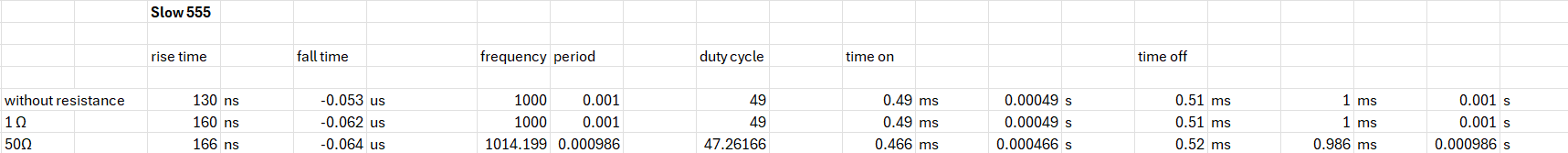
Down below are the results collected from this lab. The data sheet was also used in conjunction with the collected data in order to compare and contrast the two chips.

The slower 555 timer has a higher maximum current than the high speed 555 timer. The slower timer has a maximum current of 225 mA whereas the faster timer has a maximum current of 100 mA.

However, the slower 555 timer also has a slower rise time, as seen below, than the faster 555 timer. This means that whenever you are designing a circuit featuring a 555 timer, depending on what is prioritized in the circuit, either current output or rise time, one may select one timer over the other.

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(Fast IC datatable)

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(slow IC datatable)

A screenshot of a computer

Description automatically generated

(maximum current of fast IC)

A screen shot of a box

Description automatically generated

(max current of slow IC)

Output from both timers is down below, in the lab it was noticed that the output signal from the faster IC was lower than the output signal of the slower IC. This ties into the lower maximum current discussed before, with a lower voltage applied to the load the current output must be lower according to ohms law.

**A close up of a device

Description automatically generated**

(slower IC without load)

A close up of a device

Description automatically generated

(faster IC without load)

Before the lab the expected duty cycle and frequency was calculated via the following equations. The calculated duty cycle was expected to be 50% but it turned out only to be 30% when calculated. This is most likely due to difference in the math provided by the datasheet being based on a different configuration which featured a resistor leading into the discharge port. Further analysis could likely yield the reason why there is a difference between calculated results and measured results.

A close-up of math equations

Description automatically generated

(math used before circuit construction)

A white paper with black text and a diagram

Description automatically generated

(The differences between the circuit the math was based on vs the circuit built.)

**Conclusion**

In conclusion, this lab provided a very important lesson in trade offs in engineering. Faster ICs may provide faster rise times, at the expense of a reduced current/voltage. At the same time, slower ICS can provide higher voltages/currents, at the expense of a slower rise/fall time. It’s very important to read and pay attention to circuit diagrams before you design a circuit since there can be differences in the expected current/voltage levels.